SEMICONDUCTOR DEVICE INCORPORATED THEREIN HIGH K CAPACITOR DIELECTRIC AND METHOD FOR THE MANUFACTURE THEREOF

Field of the Invention

The present invention relates to a semiconductor device; and, more particularly, to a semiconductor memory device incorporating therein high K dielectric as a capacitor dielectric film.

Description of the Prior Art

As is well known, a dynamic random access memory (DRAM) with at least one memory cell comprised of a transistor and a capacitor has a higher degree of integration mainly by down-sizing through micronization. However, there is still a demand for downsizing the area of the memory cell.

To meet the demand, there have been proposed several structures for the capacitor, such as a trench type or a stack type capacitor, which are arranged three-dimensionally in a memory device to reduce the cell area available to the capacitor. However, the process of manufacturing three-dimensionally arranged capacitor is a long and tedious one and consequently involves high manufacturing cost. Therefore, there is a strong demand for a new memory device that can reduce the cell area with securing a requisite volume of information without requiring complex manufacturing steps.

In attempt to meet the demand, there have been introduced a high K dielectric, e.g., Ta_2O_5 or the like, as a capacitor thin film in place of conventional silicon oxide film or silicon nitride film. Since, however, a Ta_2O_5 layer is grown with a columnar structure during a following heat-treatment process, the grown Ta_2O_5 layer becomes a high leakage current. Therefore, it is very difficult for applying the Ta_2O_5 layer to a capacitor thin film for use in memory device.

Alternatively, a multi-layer dielectric, e.g., Ta_2O/TiO_2 or Ta_2O/Al_2O_3, has been proposed to use as a capacitor thin film by using a metal organic chemical deposition (MOCVD) to overcome the above-described problem. However, the MOCVD method makes a foreign material reside in the capacitor thin film. This result enforces the capacitor thin film to be performed a high temperature heat-treatment, which, in turn, generates a defect and a high leakage current in the capacitor thin film.

There are still demands for developing a high K dielectric having a low leakage current which is compatible with a semiconductor process.

Summary of the Invention

It is, therefore, an object of the present invention to provide a semiconductor device incorporating therein a high K dielectric as a capacitor dielectric.

It is another object of the present invention to provide

a method for manufacturing a semiconductor device incorporating therein a high K dielectric as a capacitor dielectric.

In accordance with one aspect of the present invention, there is provided a semiconductor device for use in a memory cell, comprising: an active matrix provided with a semiconductor substrate, a plurality of transistors formed on the semiconductor substrate and conductive plugs electrically connected to the transistors; a number of bottom electrodes formed on top of the conductive plugs; composite films formed on the bottom electrodes; and Al_2O_3 films formed on the composite films.

In accordance with another aspect of the present invention, there is provided a method for manufacturing a semiconductor device for use in a memory cell, the method comprising the steps of: a) preparing an active matrix provided with at least one transistor, a plurality of conductive plugs electrically connected to the transistors and an insulating layer formed around the conductive plugs; b) forming a conductive layer on top of the active matrix; c) patterning the conductive layer a predetermined configuration, thereby obtaining a number of bottom electrodes; d) forming a $(Ta_2O_5)_x(TiO_2)_y$ composite layer on the bottom electrodes, x and y representing a molar fraction, respectively; e) forming a dielectric layer on the $(Ta_2O_5)_x(TiO_2)_y$ composite layer; and f) patterning the dielectric layer and the $(Ta_2O_5)_x(TiO_2)_y$ composite layer into a preset configuration, thereby obtaining

the semiconductor device.

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of the preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 is a cross sectional view setting forth a semiconductor device in accordance with the present invention; and

Figs. 2A, 2B, 2C, 2D, 2E, 2F and 2G are schematic cross sectional views setting forth a method for the manufacture of the semiconductor memory device in accordance with the present invention.

Detailed Description of the Preferred Embodiments

There are provided in Figs. 1 and 2A to 2G a cross sectional view of a semiconductor device 100 for use in a memory cell and cross sectional views setting forth a method for the manufacture thereof in accordance with preferred embodiments of the present invention. It should be noted that like parts appearing in Figs. 1 and 2A to 2G are represented by like reference numerals.

In Fig. 1, there is provided a cross sectional view of the inventive semiconductor device 100 comprising an active

matrix and capacitor structures. The active matrix includes a silicon substrate 102, transistors formed on top of the silicon substrate 102, an isolation region 104 for isolating the transistors, poly plugs 116, a bit line 118 and word lines 120. Each of the transistors has diffusion regions 106, a gate oxide 108, a gate line 112 and a sidewall 114.

In the semiconductor device 100, the bit line 118 is electrically connected to one of the diffusion regions 106 to apply an electric potential. Each of the capacitor structures is electrically connected to the other diffusion regions 106 through the poly plugs 116. Although the bit line 118 actually extends in right and left directions bypassing the poly plugs 116, the drawing does not show these parts of the bit line 118. The capacitor structures can be connected to a plate line (not shown) to apply thereto a common constant potential.

Each of the capacitor structures includes a lower electrode 125, a first dielectric layer 126 formed on top of the lower electrode 125, a second dielectric layer 128, a first upper electrode layer 130 and a second upper electrode layer 132 formed on top of the first upper electrode layer 130. The second dielectric layer 128 is disposed between the first dielectric layer 126 and the first upper electrode layer 130. It is preferable that the lower electrodes 125 is made of a material selected from a group consisting of a poly silicon (poly-Si), W, WN, Wsi_x, TiN, Pt, Ru, Ir and the like and the second upper electrode layer 132 is made of a material

selected from a group consisting of a poly-Si, W, WN, Wsi_x and the like. And also, the first dielectric layer 126 is made of $(Ta_2O_5)_{0.92}(TiO_2)_{0.08}$ by using an atomic layer deposition(ALD). In the preferred embodiment, the second dielectric layer 128 is made of aluminum oxide (Al_2O_3) and the first upper electrode layer 130 is made of TiN for improving an adhesion between the second dielectric layer 128 and the second upper electrode layer 132.

Figs. 2A to 2G are schematic cross sectional views setting forth the method for manufacture of a capacitor structure 140 for use in a semiconductor memory device in accordance with the present invention.

The process for manufacturing the semiconductor device begins with the preparation of an active matrix 110 including a silicon substrate 102, an isolation region 104, diffusion regions 106, gate oxides 108, gate lines 112, a sidewall 114, a bit line 118, poly plugs 116 and an insulating layer 122, as shown in Fig. 2A. The bit line 118 is electrically connected to one of the diffusion regions 106 to apply an electric potential. Each of the poly plugs 116 is electrically connected to the other diffusion regions 106, respectively. Although the bit line 118 actually extends in right and left directions bypassing the poly plugs 116, the drawing does not show these parts of the bit line 118. The capacitor structures 140 can be connected to a plate line (not shown) to apply thereto a common constant potential. The insulating layer 122 is made of a material, e.g., boron-phosphor-silicate

glass (BPSG).

In an ensuing step, lower electrodes 125 is formed on top of the active matrix 110 by using a semiconductor process in such a way that each of the lower electrodes 125 is electrically connected to a corresponding poly plug 116, as shown in Fig. 1B. It is preferable that the lower electrode 125 is made of a material selected from a group consisting of a poly-Si, W, WN, Wsi_x, TiN, Pt, Ru, Ir and the like.

Thereafter, a first dielectric layer 126 is formed on the lower electrodes 125 and the active matrix 110 by using an atomic layer deposition (ALD). Preferably, the first dielectric layer 126 is made of $(Ta_2O_5)_x(TiO_2)_y$, wherein x and y represents a molar fraction, respectively. In the preferred embodiment, x equals to 0.92 and y equals to 0.02. The first dielectric layer 126 of $(Ta_2O_5)_{0.92}(TiO_2)_{0.08}$ can be formed by as follows: a) maintaining a reaction chamber at a temperature ranging from approximately 250 ℃ to approximately 300 ℃; b) alternatively introducing a first and a second source gases into a reaction chamber to form a Ta_2O_5 thin layer; c) alternately introducing a third and a fourth source gasses into the reaction chamber to form a TiO_2 thin layer on top of the Ta_2O_5 thin layer; d) repeating the step b) and c) to form a stacked layer of Ta_2O_5 and TiO_2; and e) heating the stacked layer at a temperature ranging from approximately 400 ℃ to approximately 550 ℃, thereby obtaining the $(Ta_2O_5)_x(TiO_2)_y$ dielectric layer.

In the embodiment, if a pentaethoxytantalum ($(Ta(C_2H_5O)_5)$ gas used as the first source gas, the second source gas can be a gas selected from a group consisting of a H_2O gas, an O_2 gas, a N_2O gas, an alcohols (C_xH_yOH) gas or the like. On the other hand, a tantalum chloride $TaCl_5$ is used as a first source gas, a second source gas can be a gas selected from a group consisting of a H_2O gas, an O_2 gas, a N_2O gas, a C_xH_yOH gas or the like. During the step b), it is preferable that the Ta_2O_5 thin layer is formed to a thickness which is less than or equal 10 Å. $TiCl_4$ is used as the third source gas and the fourth source is a gas selected from a group consisting of a H_2O gas, an O_2 gas, a N_2O gas or the like. During the step c), it is preferable that the TiO_2 thin layer is formed to a thickness which is less than or equal 5 Å. It should be noted that the step e) can be performed after the formation of upper electrodes.

It is preferable that the stacked $(Ta_2O_5)_x(TiO_2)_y$ layer has a thickness ranging from approximately 100 Å to approximately 200 Å. It should be noted that cycles of step b) and step c) are controlled in such a way that x equal to 0.92 and y equal to 0.08. After the step b), the preferred embodiment of the present invention can include the step of introducing a first inert gas into the reaction chamber for 0.1-10 seconds to remove the first and the second source gases which are remained in the reaction chamber. And also, after the step c), the formation of the first dielectric layer 126

further includes the step of introducing a second inert gas into the reaction chamber for 0.1-10 seconds to remove the source gases and the first inert gas are remained in the reaction chamber.

And, the stacked layer is patterned into a predetermined configuration, as shown in Fig. 2C.

In a following step, a second dielectric layer 128 is formed on the first dielectric layer 126, as shown in Fig. 2D. In the preferred embodiment, the second dielectric layer 128 is made of a high K dielectric material such as Al_2O_3 by using ALD.

Referring to Fig. 2E, a first upper electrode layer 130, e.g., made of TiN, is formed on top of the second dielectric layer 128 by using an ALD method for improving an adhesion between the second dielectric layer 128 and a second upper electrode layer 132 to be formed thereon. In the preferred embodiment, the ALD method utilizes $TiCl_4$ and NH_4 as a reactive source gas.

Thereafter, the second upper electrode layer 132 is formed on top of the first upper electrode layer 130, as shown in Fig. 2F. It is preferable that the second upper electrode layer 132 is made of a material selected from a group consisting of a poly-Si, W, WN, Wsi_x and the like.

And then, the second upper electrode layer 132, the first upper electrode layer 130, the second dielectric layer 128 and the first dielectric layer 126 are patterned into a memory block.

Finally, an insulating layer 150, e.g., made of BPSG, is formed on top of the capacitor structure 140 by using a method such as a plasma CVD and made flat by using a method such as chemical mechanical polishing (CMP), as shown in Fig. 2G.

By utilizing both $(Ta_2O_5)_x(TiO_2)_y$ and Al_2O_3 as a capacitor dielectric, the present invention can enhance a total dielectric constant of the capacitor dielectric with reducing a leakage current. Specifically, the total dielectric constant is increased by using $(Ta_2O_5)_x(TiO_2)_y$. And, Al_2O_3 prevent the upper electrode from reacting at an interface therebetween, thereby reducing the leakage current.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the invention as defined in the following claims.